Ka-band Direct Digital Receiver using 0.25 μm GaAs PHEMTs

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***Abstract* - A new direct conversion wideband (26GHz – 28.5 GHz) six-port millimeter wave receiver using MMIC technology is proposed to meet the needs of mass-market wireless communications. This six-port receiver is designed to operate without the need for precise power reading and the use of digital signal processor (DSP) that is usually required in other receivers. The proposed receiver architecture is chosen to satisfy requirements of hardware receiver used in QPSK communications. The receiver contains one MMIC module consisting of a wide band six-port junction with four RF Schottky detectors, a receiver front-end and a base band module composed of video amplifiers and I&Q decoder. The maximum bit rate, at least 100 Mbs, is determined solely by the limiting speed of ancillary video amplifiers and analogue decoder. This new hardware receiver is proposed as a robust, rugged, low cost receiver for use in wide Ka-band wireless mass market QPSK communications such as LMDS services that are a prime example of communication equipment requiring such receivers. BER results are presented in the presence of noise and local oscillator (LO) phase shift.**

I. INTRODUCTION

Direct conversion receivers offer unique advantages for wireless communications by reducing circuit complexity and allowing a higher level of circuit integration than the traditional heterodyne receivers [1].

Six-port direct conversion receivers have been proposed [2]-[4] as multi-mode or software receivers operated with DSP programmed for a number of modulation schemes.

This paper presents recent results obtained on a new six-port based hardware type receiver designed for QPSK communications. The proposed millimeter wave approach is also useful in the design of other hardware receivers at lower or higher operating frequencies using either discrete [3] or distributed parameter [2], [4] six-ports circuits.

The excellent results obtained with a distributed parameters six-port junction [5], [6] had a determinant role to provide an MMIC implementation of this direct digital receiver architecture.

II. RECEIVER ARCHITECTURE AND OPERATING PRINCIPLE

Figure 1 shows hardware receiver architecture composed of an MMIC module and a base-band module designed to provide I and Q demodulated signals using the four output signals of the six-port junction [5].

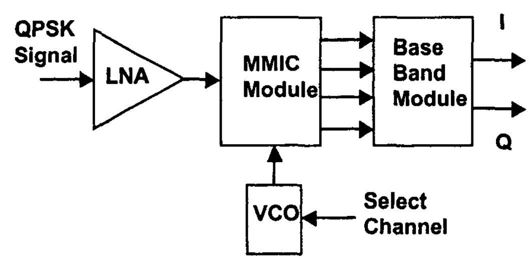

Fig.1. Receiver architecture

Figure 2 gives the topology of MMIC Module (six-port junction with RF diodes and matching circuits). The six-port junction is specially designed to demodulate a QPSK signal using three hybrid 90° couplers and a Wilkinson power divider. The relative power reading of the output signals gives sufficient information to determine the phase shift between the two RF inputs, thereby realizing a QPSK demodulator [5].

We have analyzed three different implementations for the 90° hybrid coupler in the frequency range of 24 to 30 GHz: with distributed elements, with discrete elements and a combination of both methods. The distributed elements implementation is large in size (1.39 mm^2) but it has the excellent S parameter performances. The discrete elements coupler has a very small size but the tolerances of its fabrication process at this frequency range lead to a poor S parameter performances. The hybrid implementation using high impedance transmission lines and capacities leads to very good S parameter performances.

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Figure 3 shows the RF topology of a wideband millimeter wave MMIC distributed parameter six-port junction with integrated RF Schottky diodes (marked by arrows) and their matching networks using 50 Ω transmission lines. The circuit is realized in a 100 microns GaAs substrate and its size is about 4x4 mm.

In order to reduce the size of the MMIC circuit, a new approach is proposed. The couplers are realized with the high impedance transmission lines and discrete elements (shunt capacitors of 200 fF value loaded near the ports of the hybrid couplers). The diameter of this coupler now becomes 600 microns compared with 1330 microns in the first realization. The same Schottky diode is used in the second six-port circuit. The RF Schottky diode matching networks are also realized using the shunt capacitors and high impedance transmission lines. Figure 4 shows RF topology of this new circuit. The size of this circuit is reduced to 2x3 mm, about 37% of the first six-port's size.

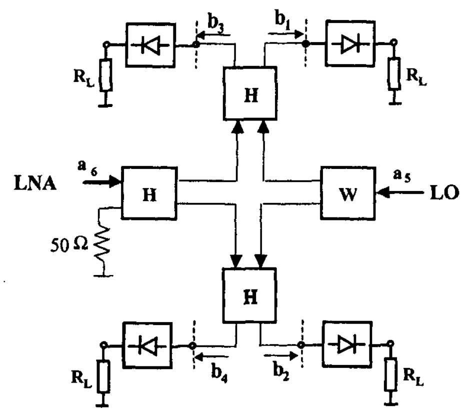

Fig.2. Six-port junction and matching detector RF circuits

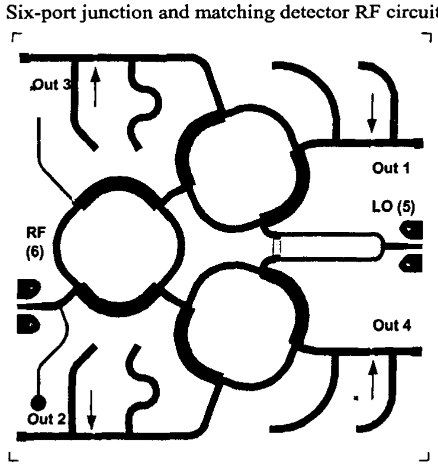

Fig.3. The distributed parameters MMIC six-port (size 4x4 mm)

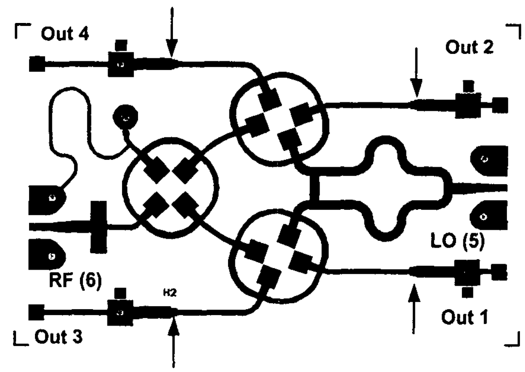

Fig.4. The hybrid implementation (distributed and discrete elements) of the MMIC six-port (size 2x3 mm)

III. Test Results

In order to characterize the MMIC six-port junction a study of its S parameters was made. The magnitude and phase of the S parameters versus the operating frequency are close to the predicted values. The results of both implementations given in Figures 3 and 4 are practically similar. In the operating band, the magnitudes of S parameters are close to the theoretical predicted values of -6 dB (Figures 5 and 6) and the phase shifts between the transmission parameters are multiples of 90° over a wide frequency band (6 GHz), as seen in Figures 7 and 8.

Figure 9 shows an excellent match at the RF inputs, and an excellent isolation between inputs (S56) in the operating frequency band for the MMIC six-port (including the Schottky diodes). Therefore the influence of DC offsets in the demodulating process is *minimized.*

The RF design of the six-port junction is such that only one of four possible modulation states is correctly identified, at any given time, by an analogue decoder. Harmonic balance simulation of the MMIC six-port is shown in Figure 10. The local oscillator (LO) and RF input power levels are both set at –3 dBm. Waveforms displayed in Fig. 10 indicate that each output voltage of the six-port junction has a single maximum value over a 360° phase-shift between RF input and LO signal. This means that Vout3, Vout4, Vout1, Vout2 have a maximum value for 0°, 90°, 180° and 270° phase shift respectively, between the input and LO signals.

The output demodulated signals versus the phase shift between RF input and LO signals as shown in Figure 11 confirms the operating principle of receiver. The four states of the output signals (11, 01, 00, 10) are obtained during a 360° phase-shift of input signal.

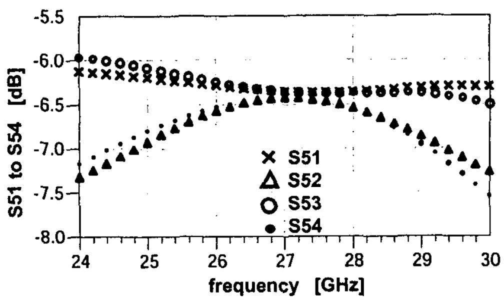

Fig.5. Magnitude of the transmission (LO to outputs) S parameters

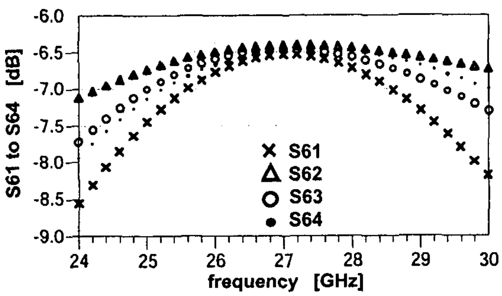

Fig.6. Magnitude of the transmission (RF to outputs) S parameters

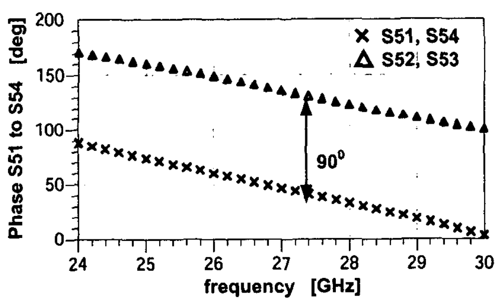

Fig.7. Phase of the transmission (LO to outputs) S parameters

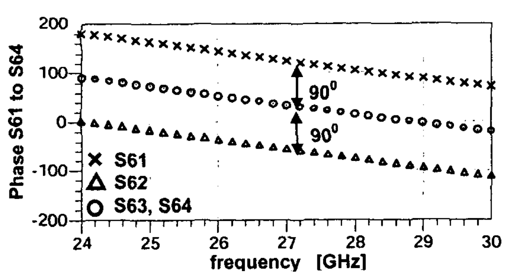

Fig.8. Phase of the transmission (RF to outputs) S parameters

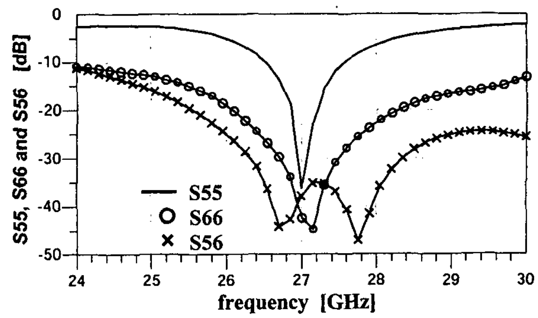

Fig.9. Adaptation and isolation at input RF ports

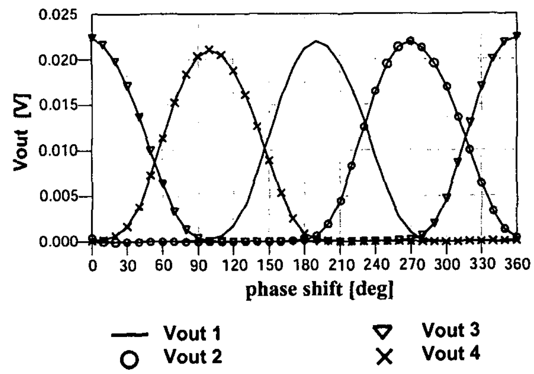

Fig.10. Output voltages of the MMIC module versus the input signals phase shift

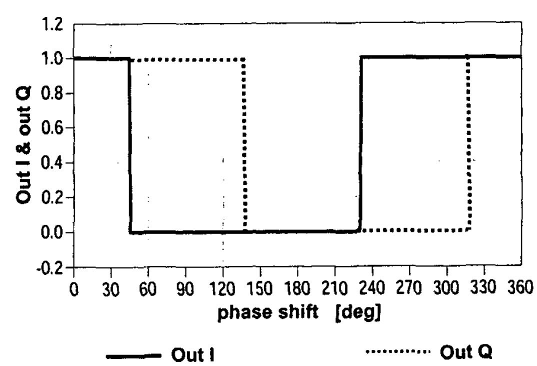

Fig.11. Output voltages of the Base Band module versus the input signals phase shift

Figure 12 shows simulated BER, as a function of E_b/N_O ratio, where E_b is the average energy of a modulated bit, and N_O is the noise power spectral density. It can be seen that at frequencies within the operating band without other perturbations, the BER curve is identically with the theoretical one for a QPSK signal. The bit rate is set at 20 Mb/s and the LO power is –3 dBm.

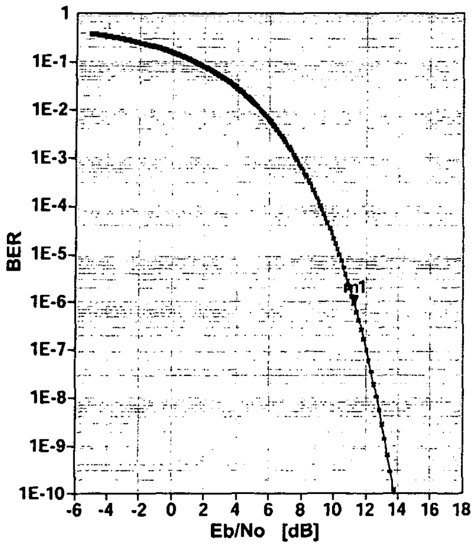

Fig.12. Simulated BER vs. Eb/No at 27 GHz

Figure 13 shows the simulated BER versus the LO phase error from synchronism (0 deg) at 27 GHz.

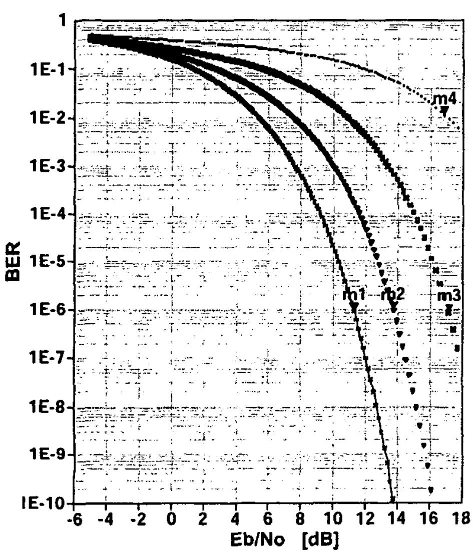

Fig13. Simulated BER vs. LO phase error from synchronism

The four curves are for the phase error less than 20° (m1), 20° (m2), 30° (m3) and 40° (m4). Therefore, this six-port MMIC QPSK demodulator has a very good tolerance to phase noise as well.

IV. Conclusions

A new direct conversion hardware receiver based on six-port technology suitable for LMDS applications was presented. The six-port circuit of this receiver was integrated in 0.25 μm GaAs PHEMT Technology at TriQuint Semiconductor Foundry.

Acknowledgements

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References

[1] A. A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications", *Journal of Solid- State Circuits*, vol. 30, no. 12, pp.1399- 1410, December 1995

[2] J. Li, R.G. Bosisio, K. Wu, "Computer and Measurement Simulation of a New Digital Receiver Operating Directly at Millimeter-Wave Frequencies", *IEEE Transactions. Microwave Theory & Technique*, vol.43, no.12, pp. 2766-2772, December 1995.

[3] M. Abe, N. Sasho, V. Brankovic, and D. Krupezevic, "Direct Conversion Receiver MMIC Based on Six-Port Technology", *European Conference on Wireless Technology ECWT 2000, Conference Proceedings*, pp. 139-142, October 2000.

[4] J. Hyryläinen, L. Bogod, "Six Port Direct Conversion Receiver", *European Microwave Conference Proceedings*, pp. 341-347, September 1999.

[5] S.O. Tatu, E. Moldovan, Ke Wu, R.G. Bosisio, "A New Direct Millimeter-Wave Six-Port Receiver", *IEEE Transactions on Microwave Theory and Techniques*, vol.49, no.12, pp 2517-2522, December 2001.

[6] S.O. Tatu, E. Moldovan, Ke Wu. R.G. Bosisio, "A New Carrier Recovery Method for a Six-Port Millimeter-Wave Receiver", *ISMOT 2001, Conference Proceedings*, pp.211-214, June 2001